REMARKS

Applicants believe the Examiner has made a premature Final Rejection. In Applicants response of December 27, 2005, Applicants noted that claim 14 had not been Examined. Applicants requested an examination of claim 14. The examiner has responded that "the limitations of claim 14 were addressed in the rejection of claim 7." Applicants contend Applicants had no way of knowing the Examiners intentions regarding claim 14 and that the Examiner is under obligation to examine each and every claim and indicate reasons for rejection of each and every claim. By not doing so, as regards claim 14, Applicants were denied an opportunity to respond fully. The Examiner is penalizing Applicants for an attempt to respond as best they could in light of the Examiners error by making the current rejection final. Therefore, Applicants, respectfully request the Examiner width draw the finality of the May 14, 2006 office action.

Applicants have amended claim 26 to correct a typographical error and not in response to the Examiners rejection of claim 26.

The second claim 22 was misnumbered and has been renumbered 26.

Applicants believe the amendments of claims 1, 8 and 26 will put the application in better form for appeal and request the amendments of claims 1, 8 and 26 be entered.

The Examiner rejected claim 8 under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

The Examiner rejected claims 1, 8 and 15 under 35 U.S.C. 112 (second paragraph) as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

The Examiner rejected claims 1, 3-6, 8, 10-15, 17-20 and 30 under 35 U.S.C. 102(e) as being anticipated by Evans et al. (U.S. Patent 6,279,146).

The Examiner rejected claims 2129 under 35 U.S.C. 103 as being unpatentable over Evans in view of Dutta et al. "Viper."

Applicants respectfully traverse the §101, §112, §102 and §103 rejections with the following arguments.

35 USC § 101 Rejections

The Examiner rejected claim 8 under 35 U.S.C. 101 "because the claimed invention is directed to non-statutory subject matter." The Examiner further stated "Claim 8 recites a software method. It is unclear how a method, which is a set of steps, can also be a piece of software. Software does not comprise steps, but rather a sequence of code that when executed can perform a set of steps. Claim I is not rejected under 35 U.S.C. 101 as it does recite an actual device."

Applicants, have amended the preamble of claim 8 to clearly indicate that a method, not software is being claimed.

35 USC § 112 Rejections

The Examiner rejected claim 1 under 35 U.S.C §112, second paragraph stating: "Claim 1 recites a software system but includes an external memory mapped test device which is hardware. It is unclear how the system can be software if an element of the system is embodied as hardware." In response, Applicants have amended claim 1, to indicate that the external memory mapped test device (EMMTD 170) is a software module.

Applicants point to Applicants page 11, lines 9-22 which states "For the purposes of the present invention, SOC 100 is intended to include embodiments in any known form of logic design, including simulatable HDL modules and netlists. In one example, embedded processor core 105, memory controller core 110, dedicated 1394 core 115, dedicated UART core 120, muxed serial core 125, muxed UART core 130, muxed DMA core 135, GPIO core 140, external memory model 165, **EMMTD 170**, dedicated 1394 model 175, dedicated UART model 185, muxed UART model 210, muxed serial model 225 and muxed DMA model 240 are HDL modules being simulated by a test operating system (TOS) and memory bus 160, GPIO bus 205 and buses 145, 150, 155, 180, 190, 215, 220, 230, 235, 245, 250 and 255 represent virtual connections implemented by code specifications."

The Examiner rejected claim 8 under 35 U.S.C §112, second paragraph stating: "Claim 8 recites a software method but includes an external memory mapped test device which is hardware. It is unclear how the method can be software if an element of the system is embodied as hardware."

In response, Applicants have amended claim 8, to remove the word "software" from the preamble of claim 8.

Applicants point out that claim 8 recites "an external memory mapped test device software module" which is clearly not hardware as the Examiner alleges and is clearly described in Applicants specification as one of the "HDL modules being simulated by a test operating system." See response to first §112 *supra*.

The Examiner rejected claim 8 under 35 U.S.C §112, second paragraph stating Claim 8 recites a software method. It is unclear how a method, which is a set of steps, can also be a piece of software. Software does not comprise steps, but rather a set of code that when executed can perform a set of steps.

Applicants, have amended the preamble of claim 8 to clearly indicate that a method, not software is being claimed.

The Examiner rejected claims 1, 8 and 15 under 35 U.S.C §112, second paragraph stating " Claims 1, 8, and 15 recite 'programmably connectable.' It is unclear what is meant by programmably connectable. It is unclear if this is hardware or software connected to another piece of hardware or software. Please refer to the specification when responding to the rejection."

Applicants point to page 17, line 20 to page 18 line 4 which states "For the purposes of the present invention, **EMMTD 170A (including address register 312 and switch 315)**, muxed UART model 325, muxed serial model 340 and muxed DMA model 355 are HDL modules being simulated by the TOS and buses 320, 330, 335, 345, 350, 360, 365 and 370 represent virtual connections implemented by code specifications" and to page 18, lines 16-21 which state

"**EMMTD switch 315 is also programmed to selectively connect** bus 320 to bus 330 allowing muxed UART model 325 to be connected to EMMTD 170A and address register 312. EMMTD switch 315 allows one model to take control of GPIO bus 205. EMMTD switch 315 is a controlled by the TOS and eliminates the need for tri-state control." The Examiner is also directed to page 3, lines 12-13 where it HLD is clearly indicated as a software language, to wit "software written in hardware description language (HLD)."

Clearly, the EMMTD switch is a software module (HDL module) virtually connected to I/O driver modules which are also software modules.

Applicants maintain, based on the previous arguments, that claim 1 (as amended) and claims 8 and 15 are not rejectable under 35 U.S.C. 112 (second paragraph) and are in condition for allowance. Since claims 3-6 and 21-23 depend from claim 1, claims 10-13, 24-26 and 30 depend from claim 8, and claims 17-20 and 27-29 depend from claim 15, Applicants contend that claims 3-6, 10-13, and 17-30 are also allowable.

35 USC § 102 Rejections

As to claims 1. 8 and 15:

First, Applicants respectfully point out, Applicants are teaching a **software simulator** for testing a design and that the only hardware in Applicants claimed invention is the test system running the test operating system (TOS). All other elements are software models or software modules under the control of the test operating system when a test case, which is a set of instructions, is loaded onto the test operating system.

By contrast, Evans is teaching a **hardware modeler** for testing a design as evidenced by: (1) Evans col. 2, lines 42- 50 which states "Hardware modelers address the above noted problematic situation in which a net list does not exist for one of the target system blocks. In this situation it is generally the case that a physical embodiment of the block exists in the form of an IC or a bonded IC core (a portion of an IC that has been extracted and equipped with connector pins). A hardware modeler is designed to connect such a physical embodiment to a computer executing a simulation model ('a simulator')."

(2) Evans col. 4, lines 1-8 which states 'In a first preferred aspect, the present invention is a verification engine for verifying the design of a target system having a plurality of components interconnected by a plurality of target system buses. The verification engine comprises a first hardware model and a second hardware model, both configured as a said component and having a set of hardware model input/output pins."

Clearly Evans is teaching hardware not software and cannot constitute prior art under 35 U.S.C. 102(e) because the Evans et al. does not describe Applicants invention.

Second, using the Examiners claim 1 rejection as exemplary for claims 8 and 15:

As to Evans' external memory mapped test device, Applicants point out that FIG. 5 is a functional block diagram of a core card of FIG. 4 not a "software module" as Applicants claims 1, 8 and 15 require. Evans FIG. 4 is a "a physical side view of the preferred apparatus embodiment of the present invention."

As to Evans' I/O driver models, I/O controllers, I/O driver modules and simulated I/O cores, none of these is taught in Evans col. 10 line 60 to col. 11 line 26. Only the bus wrapper configuration is taught.

As to Evans' virtual memory bus, in Evans col. 10 line 60 to col. 11 line 26 the bus wrappers are hardware that "serve the function of more than one virtual bus wrapper for more than one virtual bus." (see also Evans col. 4, lines 12-17 which indicate the bus wrappers include "circuitry."

Based on the preceding arguments, Applicants respectfully maintain that claims 1, 8 and 15 are not unpatentable over Evans et al. and are in condition for allowance. Since claims 3-6 and 21-23 depend from claim 1, claims 10-13, 24-26 and 30 depend from claim 8, and claims 17-20 and 27-29 depend from claim 15, Applicants contend that claims 3-6, 10-13, and 17-30 are likewise in condition for allowance.

35 USC § 103 Rejections

First, as to claim 21-29, Applicants have argued *supra* in response to the Examiners § 102(e) rejection of claims 1, 8 and 15 that claims 1, 8 and 15 are allowable, since claims 21-23 depend from claim 1, claims 24-26 depend from claim 8 and claims 27-29 depend from claim 15, Applicants respectfully maintain that claims 21-29 are not unpatentable over Evans et al. in view of Dutta et al. and are in condition for allowance.

Second, Applicant maintain the rejections are improper because there is no suggestion in the prior art to combine the references as required by *Karsten Mfg. Corp. v. Cleveland Gulf Co.*, 242 F.3d 1376, 1385, 58 U.S.P,Q.2d 1286, 1293 (Fed. Cir. 2001) which states " In holding an invention obvious in view of a combination of references, there must be some suggestion, motivation, or teaching in the prior art that would have led a person of ordinary skill in the art to select the references and combine them in the way that would produce the claimed invention." The alleged motivation does originate from prior art but has been supplied by the Examiner. Therefore, the Examiner has not established his prima facie case of obviousness.

Applicants also take exception to the Examiners statement that "the types of cores refer to intended use." Applicants maintain that the "cores" are software models that are being tested by simuation not an intended use of the cores.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,
FOR:
Devins et al.

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